Customer No.: 31561
Docket No.: 13530-US-PA
Application No.: 10/711,473

REMARKS

Present Status of the Application

The Office Action rejected claims 1, 2, 6, 12, 18 and objected claims 1-3, 5-8, 10-13 and 15-17. Specifically, the Office Action rejected claims 1, 2, 6, 12, 18 under 35 U.S.C. 103(a) as being unpatentable over Shih (US 2003/0230748) in view of Song (U.S. 5,990,986) and further in view of Peng (US 2004/0219723). Applicants have amended claims 1, 12 to overcome the rejection. After entry of the foregoing amendments, claims 1-18 remain pending in the present application, and reconsideration of those claims is respectfully requested.

Discussion of Office Action Rejections

Applicants respectfully traverse the rejection of claims 1, 2, 6, 12 and 18 under 103(a) as being unpatentable over Shih (US 2003/0230748) in view of Song (U.S. 5,990,986) further in view of Peng (US 2004/0219723) because a prima facie case of obviousness has not been established by the Office Action.

To establish a prima facie case of obviousness under 35 U.S.C. 103(a), each of three requirements must be met. First, the reference or references, taken alone or combined, must teach or suggest each and every element in the claims. Second, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skilled in the art, to combine the references in a manner resulting in the claimed invention. Third, a reasonable expectation of success must exist. Moreover, each of the three

requirements must " be found in the prior art, and not be based on applicant's disclosure." See M.P.E.P. 2143, 8th ed., February 2003.

The present invention is in general related a low temperature polysilicon thin film transistor and a method of fabricating a lightly doped drain region as claims 1 and 12 recite:

Claim 1. The low temperature polysilicon thin film transistor, comprising:
a substrate;
a polysilicon layer, disposed over the substrate, the polysilicon layer comprising a lightly doped drain, a channel region inside the lightly doped drain region and a source/drain region outside the lightly doped drain region;
a gate insulation layer, disposed over the substrate covering the polysilicon layer;
a gate buffer layer, arranged over the gate insulation layer covering the channel region and the lightly doped drain;
a gate, disposed over the gate buffer layer covering the channel region, ***and the gate buffer layer is disposed between the gate and the gate insulation layer***;
a dielectric layer, arranged over the gate insulation layer covering the gate;
a drain metal layer, disposed over the dielectric layer and through the dielectric layer and the gate insulation layer to electrically connect with the drain region; and
a source metal layer, disposed over the dielectric layer and through the dielectric layer and the gate insulation layer to electrically connect with the source region.

Claim 12. The method of fabricating a lightly doped drain region, comprising:
forming a polysilicon layer over a substrate;
forming a gate insulation layer over the polysilicon layer;
sequentially forming a gate buffer layer over the gate insulation layer and a gate over the gate buffer layer ***so that the gate buffer layer is formed between the gate and the gate insulation layer***, wherein an edge portion of the gate buffer layer is exposed; and
performing a doping process to form a lightly doped drain region in the polysilicon layer underneath the exposed portion of the gate buffer layer.

Song fails to teach or suggest that the gate buffer layer is disposed or formed between the gate and the gate isolation layer. In Song's reference, a TFT, as shown in Fig. 3, comprises a gate consisting of an Al alloy layer 111 and a Mo layer 112, a gate insulating layer 20 covering the gate, an amorphous silicon layer 30 over the gate insulating layer 20, a buffer layer 51, 52

over the amorphous silicon layer 30 and a transparent conductive layer 61, 62. In particular, the buffer layer 51, 52 is formed over the gate and the gate insulating layer 20. However, Song does not teach or suggest that a gate buffer layer is formed between the gate and the gate insulating layer as claims 1, 12 recite.

The office Action points out that Shih fails to disclose the gate buffer layer over the gate insulating layer. But Song also fails to teach or suggest ***the gate buffer layer that is*** arranged over the gate insulation layer covering the channel region and the lightly doped drain and ***disposed between the gate and the gate insulation layer*** as claim 1 recites. Song also fails to teach or suggest that the step of sequentially forming a gate buffer layer over the gate insulation layer and a gate over the gate buffer layer ***so that the gate buffer layer is formed between the gate and the gate insulation layer***, wherein an edge portion of the gate buffer layer is exposed as claim 12 recites. Hence, Song cannot cure the deficiencies of Shih.

For at least the foregoing reasons, Applicant respectfully submits that independent claims 1 and 12 patently define over the prior art references, and should be allowed. For at least the same reasons, dependent claims 2-11, 13-18 patently define over the prior art as well.

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CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 1-18 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

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